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B. E. (Third Semester) Examination, April-May 2020

(New Scheme)

(CSE Branch)

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allowed: Three hours

Maximum Marks: 80

Minimum Pass Marks: 28

Note: Attempt all questions. Part (a) of each unit is compulsory and carries 2 marks. Attempt any two parts from part (b), (c) and (d) of each unit. (Imarks each)

POPPE Unit-I

- 1. (a) What is Gray code?
 - (b) A 7-bit Hamming code is received is 0010001.

 Assuming that even parity has been used, check

if it is correct. If not find the correct code, if parity is used.

- (c) State and explain De-Morgan theorem of between algebra.
 - (d) Simplify the Boolean function using *K*-map

$$f = \sum m(0, 2, 3, 8, 10, 12) + d(4, 6, 7)$$

Also draw its logic gate.

Unit-II

- 2. (a) What is Tri state logic?
 - (b) What do you mean by TTL with its totem pole arrangement?
 - (c) Explain various parameter of digital logic family in brief.
 - (d) Explain interfacing of TTL to CMOS and CMOS to TTL.

1000200 at Light from Unit-III running Hard 1 stands

- 3. (a) Define multiplexer with its diagram.
 - (b) Draw and explain function of full-adder circuits.
 - (c) Implement a 3 line to 8 line decoder with its logic diagram.
 - (d) Explain octal to binary encoder with its working.

Unit-IV

- **4.** (a) What is sequential circuit?
 - (b) Convert the SR ff to JK ff.
 - (c) Explain T-ff with its working.
 - (d) Draw and explain parallel in serial at shift register.

Unit-V

- 5. (a) Define ROM.
 - (b) Werite down the classification and characteristics of various types of memory.
 - (c) Explain the function of PLA.

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(d) What are the different application of ROM?	
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Converting SR Bro JK B:	
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